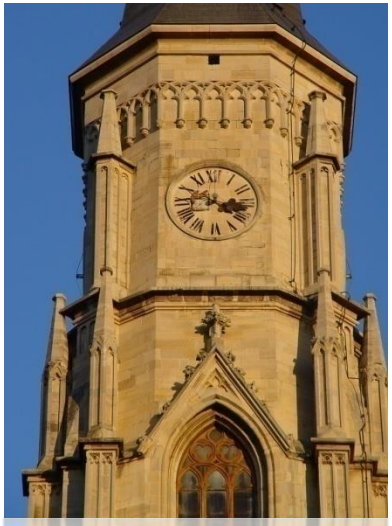
EUROPEAN UNIVERSITY OF TECHNOLOGY

TECHNICAL UNIVERSITY OF CLUJ-NAPOCA



DERFAIC
the “Digitally Enhanced RF and Analog ICs” Research Group

Assoc. Prof. Marius Neag

Overview

- Microelectronics R&D activities @ Derfaic Group
  - Team, resources and areas of expertise
  - Design of Analog & Mixed-Signal ICs and Systems
  - IC Characterization, Modelling, Multivariate yield analysis
  - Sample projects: Arpic1; AFE for automotive Hall sensor; the “Home Electronic Laboratory”
- Recent industry-related R&D projects
  - The PartEnerIC project within the POC framework
    - ✓ Brief description & Main results
    - ✓ Example of a PMIC developed: Ultra-Low (<1uA) LDO
  - The iDev4.0 project within the Ecsel framework
    - ✓ Brief description & Main results
    - ✓ Design methodologies for PMICs based on electro-thermal simulator
- Plans for future co-operation with industry

"Digitally Enhanced RF and Analog IC" Group – DERFAIC Research Group

http://icdesign.utcluj.ro

Competences:

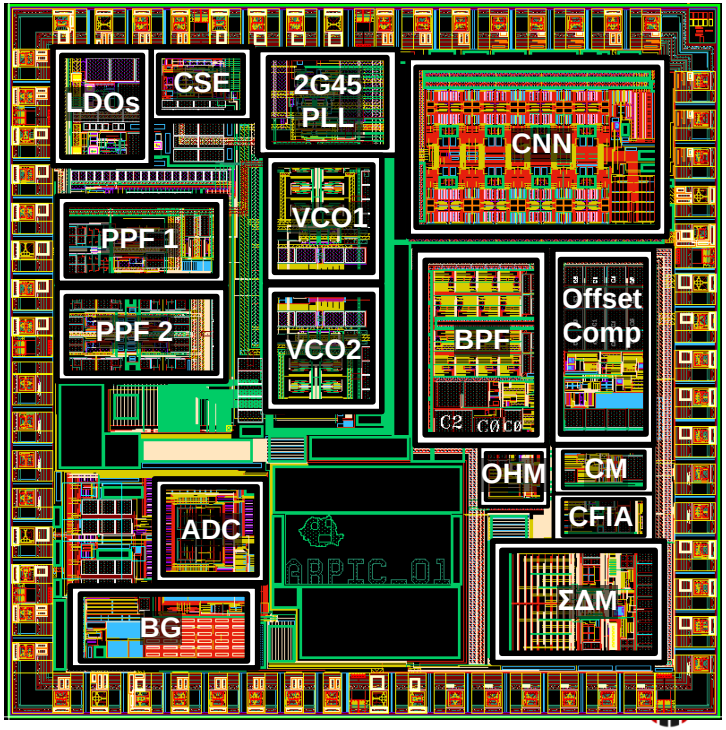
- Design of RF, Analog and Mixed–Signal Integrated Circuits
- Machine Learning for post-Si verification and big data analysis; yield analysis and prediction, yield detractors
- Methodologies for systematic and optimized IC design
- Digital techniques for enhancing analog IC performance
- Statistical analysis and testing of integrated circuits & systems
- Electronic circuits and systems for acoustics

Team:

- 8 staff members
- 2 post-doc researchers
- 6 PhD students
- 4 Undergraduate & 1 Master students with scholarships from industry

Labs and Affiliations:

- 2 research labs
- access to 3 general-purpose electronics labs
- access to EMC lab and anechoic enclosure
- own farm of simulation servers
- Cadence Academic Network affiliation since 2010
- Europractice membership
- Romanian Academic Platform for IC Development



DERFAIC – IC design and silicon implementation

Power Management ICs

Linear

- LDOs with fast response to load transients
- “Any Cload” LDOs
- Low-power **Voltage references and regulators**
- Start-up circuits
- **Current sensing**

Switched-Mode

- Switched-Cap DC-DC converters
- Inductor-based DC-DC converters for light loads
- Digital control for SMPS

Analog Front-Ends

Amplifiers

- LNA, instrument amplifiers
- Programmable-gain & constant BW
- Power Buffers

Continuous-time Filters

- Very low and very high frequency
- Tunable/programmable/re-configurable

Frequency synthesis

Functional blocks for GHz apps.

- LC- and ring-VCOs
- Programmable frequency dividers

Fast-lock Integer-N PLLs

- Frequency comparators
- Early-late detector

RF ICs - Transceivers for wired and wireless comms.

Radio transceivers

- LNAs and Mixers
- Base-band circuitry
- Tx PPA

Transceivers for wired communications

- Rx and Tx analog interfaces
- Clock generation and clock recovery

DERFAIC – Systems with ICs

Power Management

Low-power

- SMPS based on SC DC-DC converters +LDOs
- SMPS with digital control
- Inductive power transfer

Renewable

- MPPT control for PWM-based DC-DC converters

Power Quality

- Systems for power quality factor correction

Transceivers

Wearable sensors

- Low-power Rx and Tx
- Analog signal processing
- Example: Wearable health monitors with TransferJET data transfer

Impedance-based sensors

- Rx and Tx analog circuitry
- Apps in geology, food safety and health

Sensors

Bias and control circuitry

- CMOS drivers for MEMS body-biasing
- CMOS drivers for MEMS control

AFE

- Instrument amplifiers
- Continuous-time filters

Acoustics

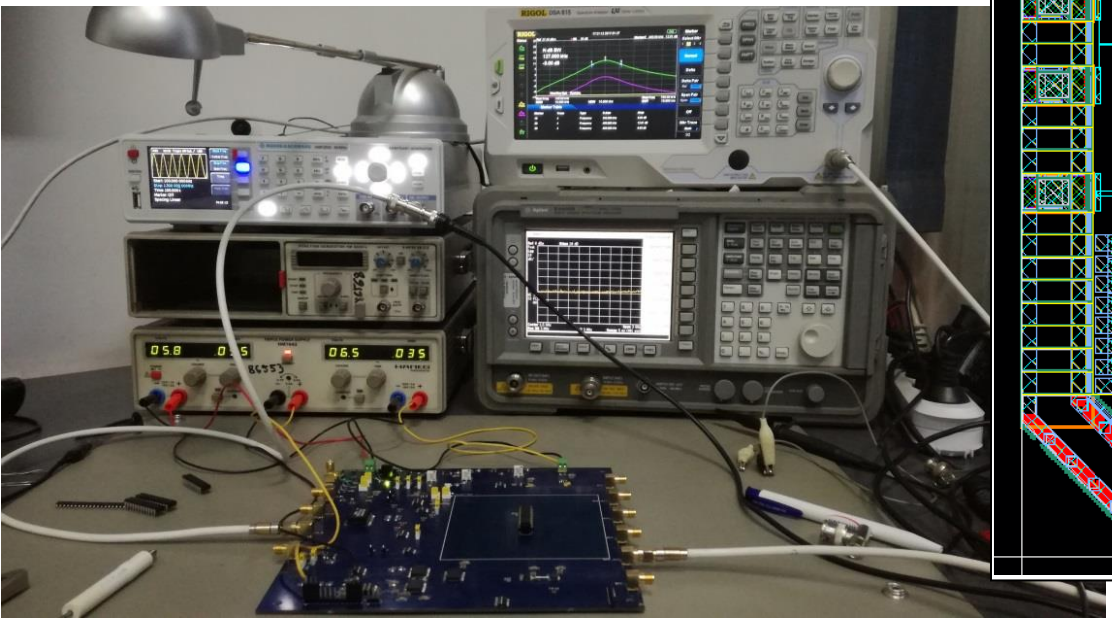
Equalizers for hearing aids

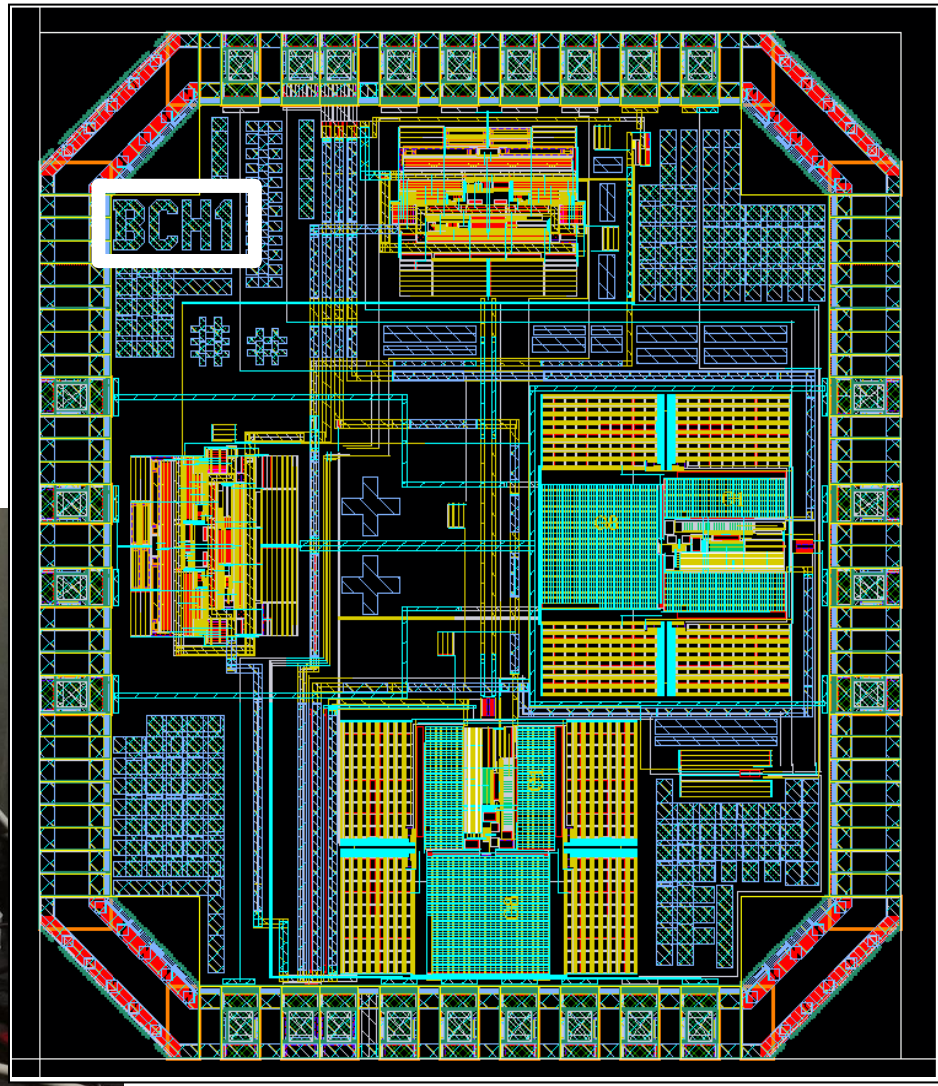
Equalizers for medium- to large-volume enclosed spaces

Modelling acoustic features of various enclosures

Examples of IC Design Projects
AFE for automotive Hall sensor

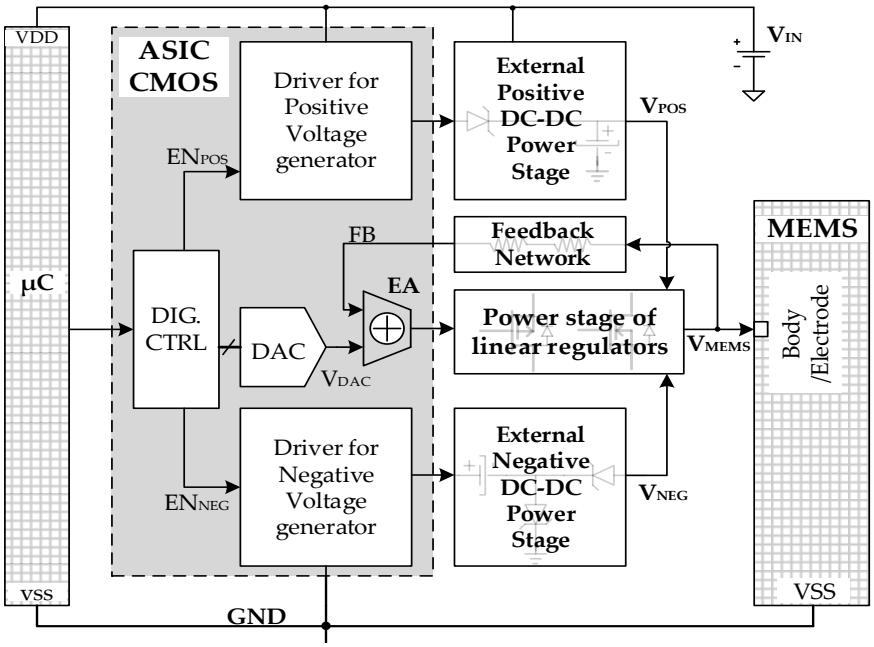
- **ASIC design :** two versions of LNA + BPF, 0.18 um CMOS
- **Design of test platform**
- **Complete characterization,** including noise sensitivity



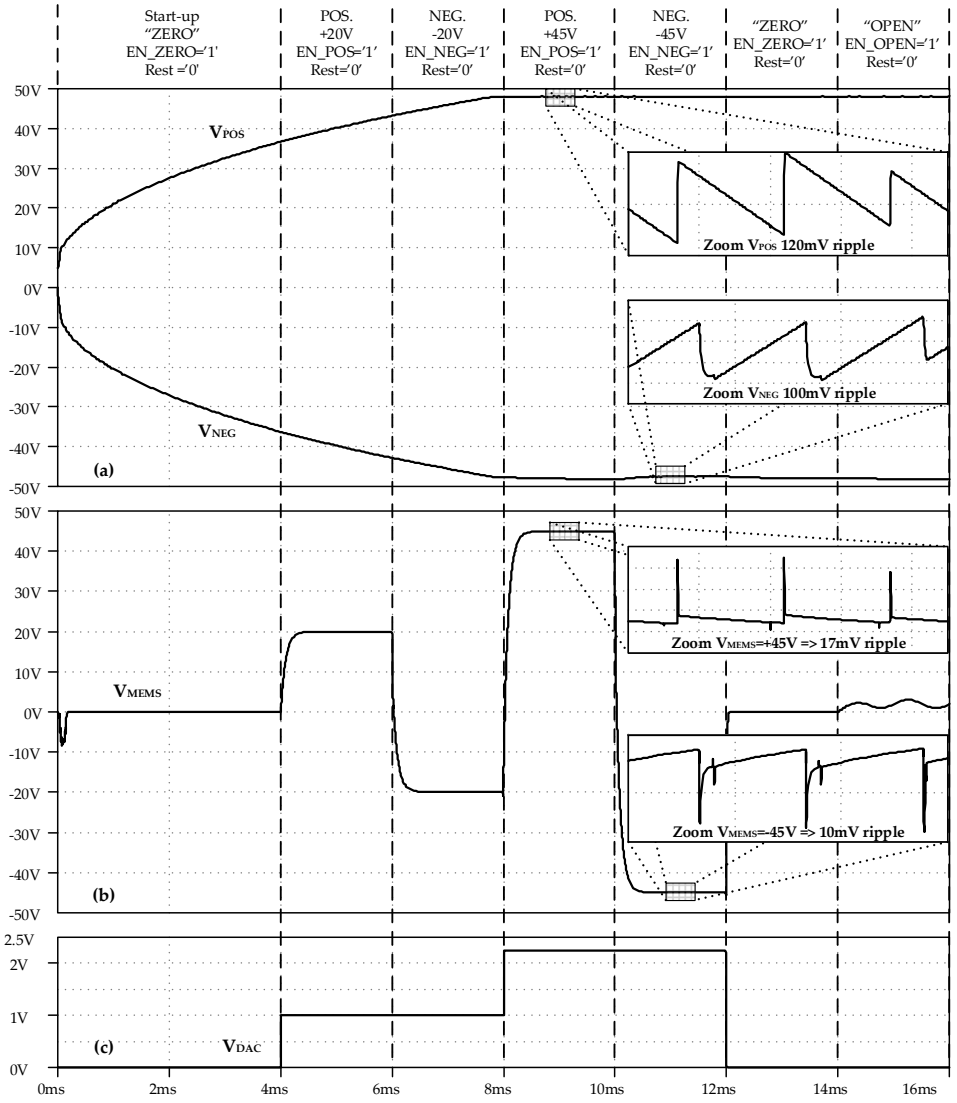


Examples of IC Design Projects: Standard CMOS One-ASIC Drivers for MEMS sensors and actuators

- **Topology**



- **Sim Results**



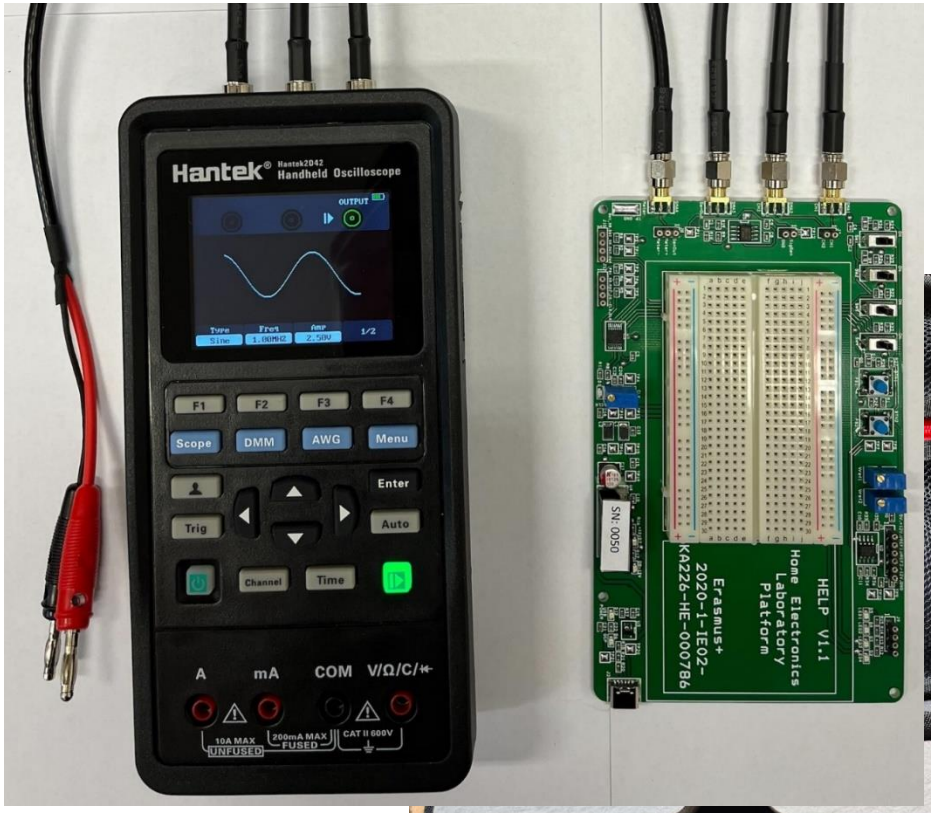
- **Four operation modes:**

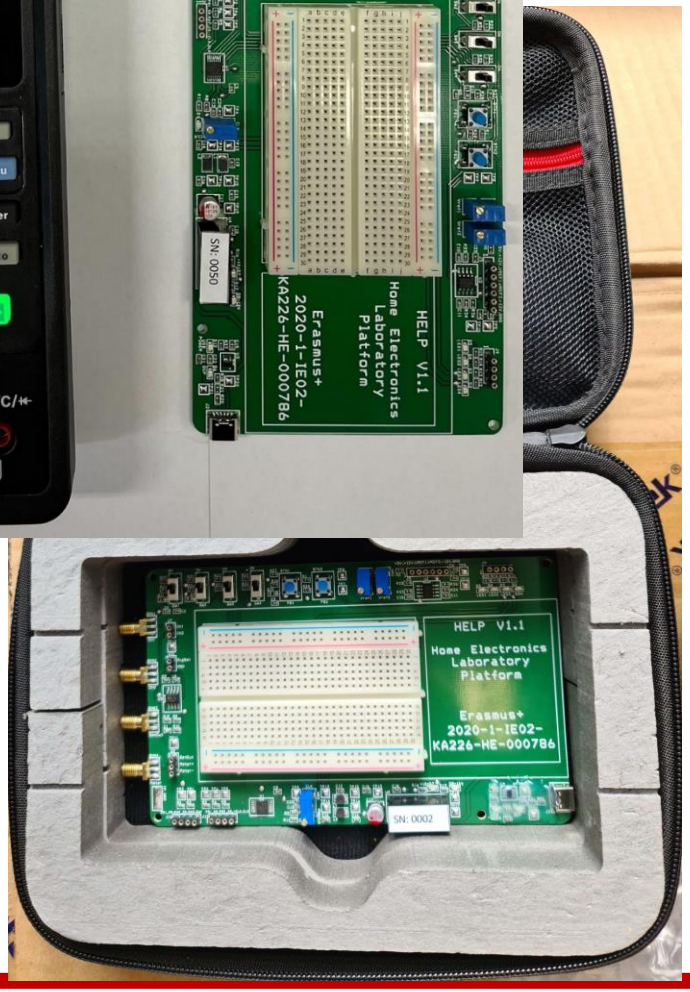
"NEG" and "POS" : outputs V_{MEMS} programmable between [-45V, 0] and [0, +45 V], with a resolution of 200mV

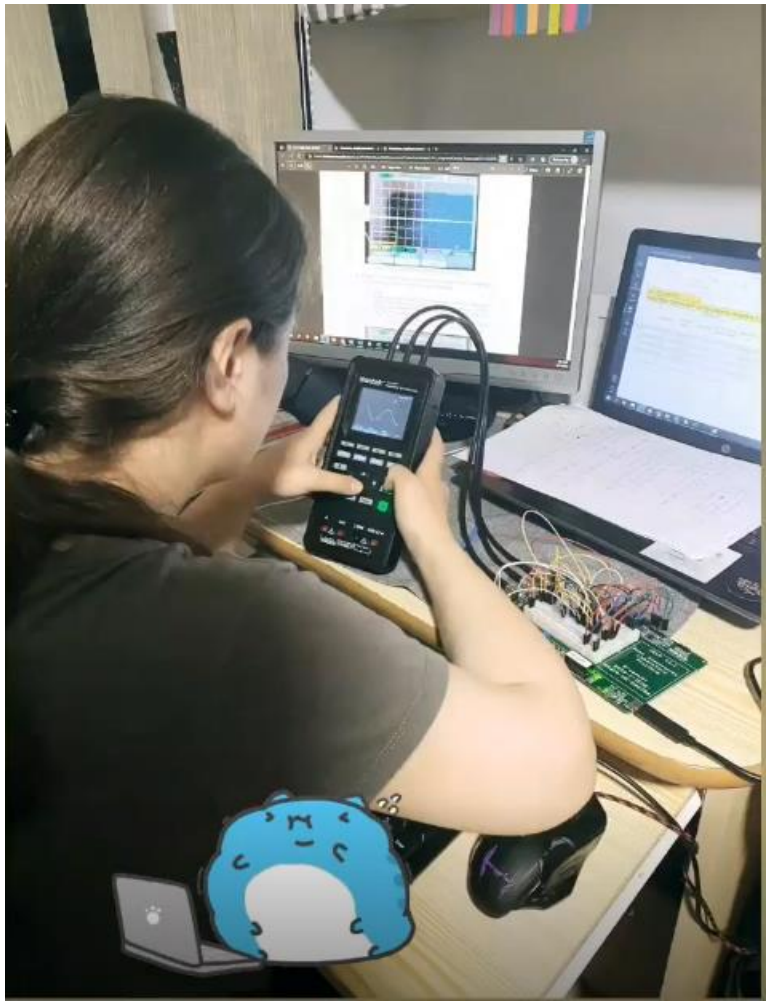
"Zero" : output shorted to GND

"Open": output left floating

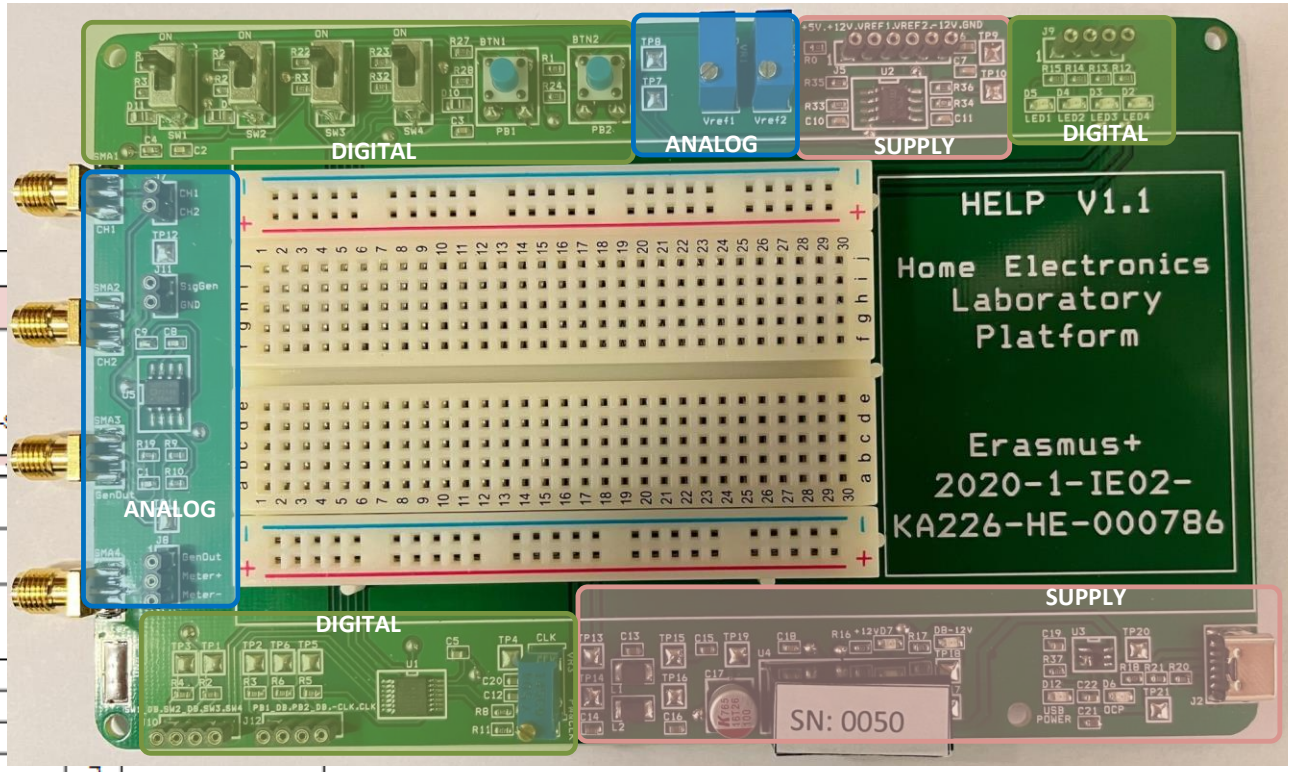
The Home Electronics Laboratory
HELP kit = Lab-in-a-bag

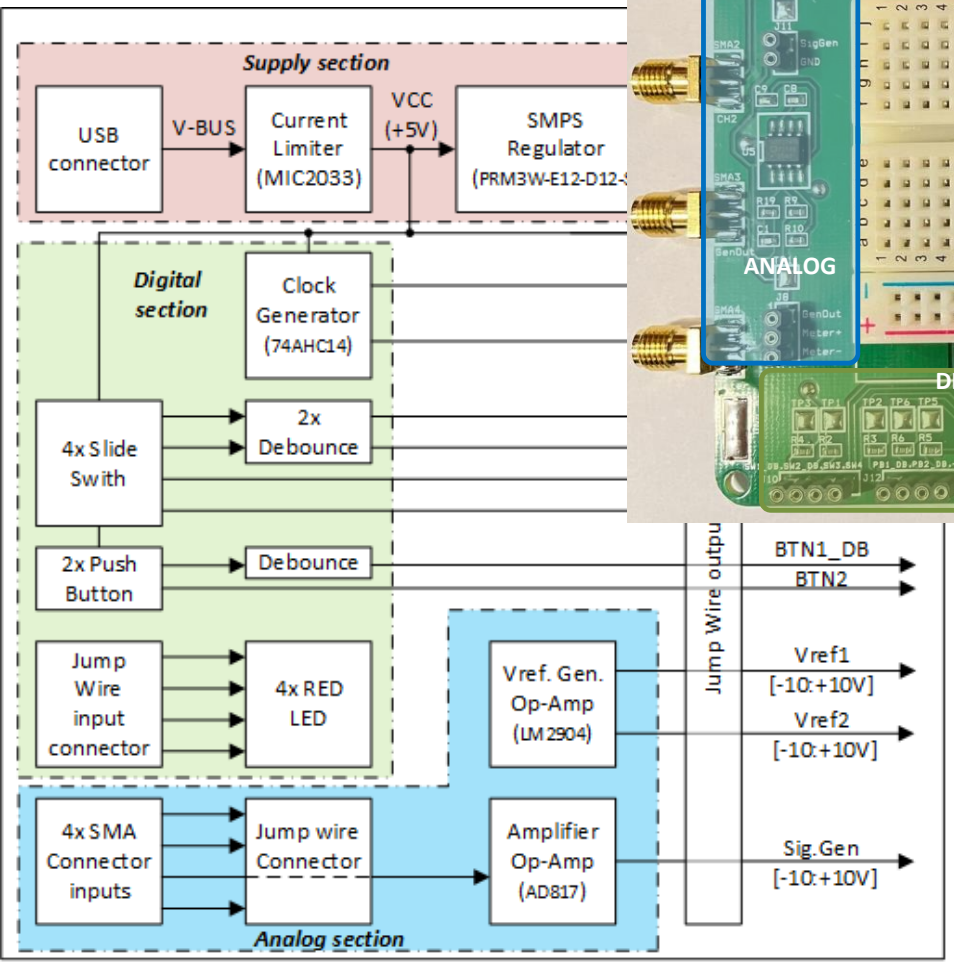






The Home Electronics Laboratory
HELP kit electronic board





Main recent EU-funded projects (+2.5Million Euro)

The PartEnerIC project – https://parteneric.utcluj.ro/

Aim: R&D in Methodologies for design, optimization and statistical analysis of Power Management ICs for, and in collaboration with, industrial partner = Infineon Technologies
Duration: 5 years (2016-2022) **Budget:** 2+ million Euro (10.1 million RON)

Main Results:

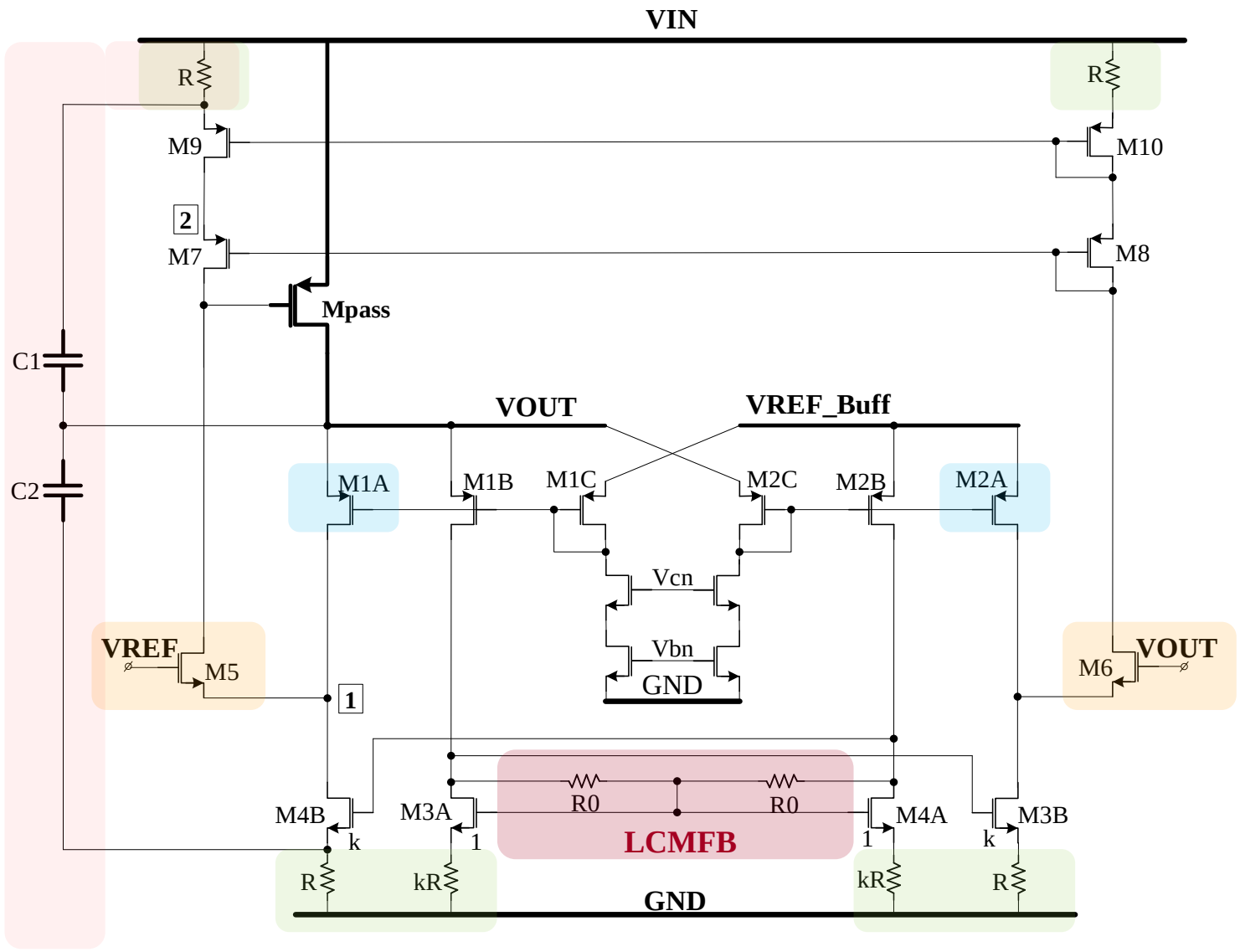
- 7 test-chips comprising 9 LDOs, 3 DC-DC converters & several functional blocks such as: current sense, start-up, bandgaps
- New machine learning-based methodologies for verification, characterization and modeling of LDO/DC-DC integrated circuits
- New methodologies for systematic and optimized design of PMICs
- 3 PhD theses completed; 29 papers published, of which 17 in ISI journals
- 3 patent applications, one already granted by the German Patent and TM Office

The Integrated Development 4.0 project – http://www.idev40.eu/

Consortium of 20+ partners from 6 EU countries, led by Infineon Technologies
Duration: 2.5 years (2019-2022) **Budget:** 500K+ Euro
Main Results:

- Novel methodologies for yield analysis & prediction, identification of yield detractors
- Methodologies for Multiphysics (Electro-Thermal-Mechanical) Analysis of Power ICs
- 1 PhD thesis completed; 10+ papers published, of which 4 in ISI journals

The PartEnerIC project: Ultra-low power LDO in 0.18um CMOS

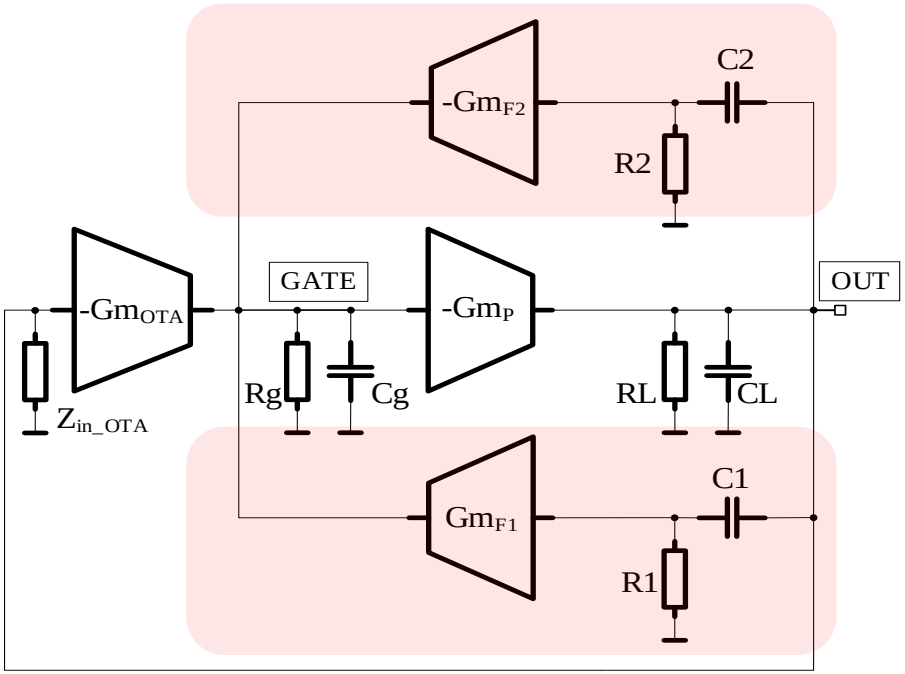


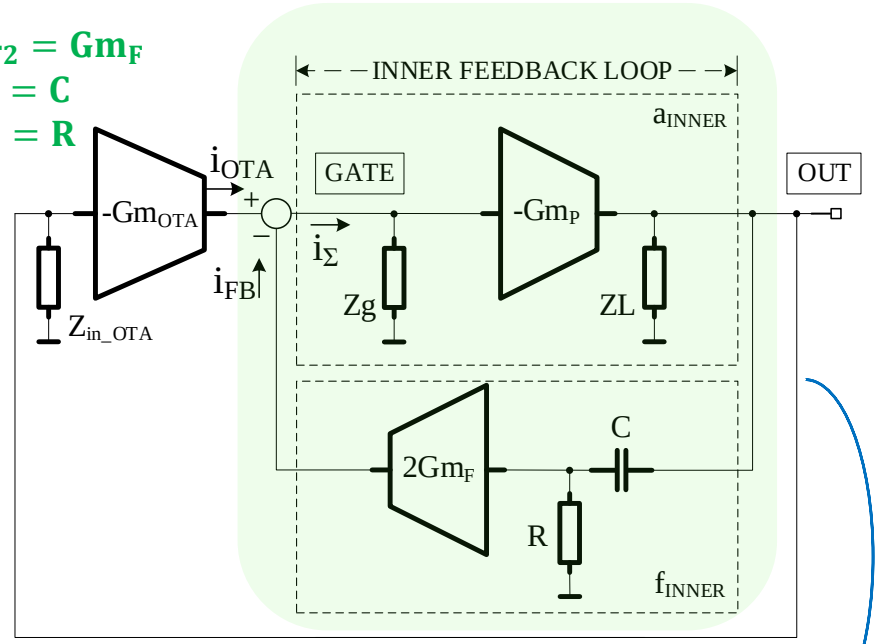
LDO highlights:

- Iq=0.7uA
- wide range of Cload (0 to 1uF)
- Iout:0 to 100mA
- ΔVout_pkpk for Iload 0 to 100mA < 275mV
- VIN:1.2V – 1.5V
- VOUT=1V

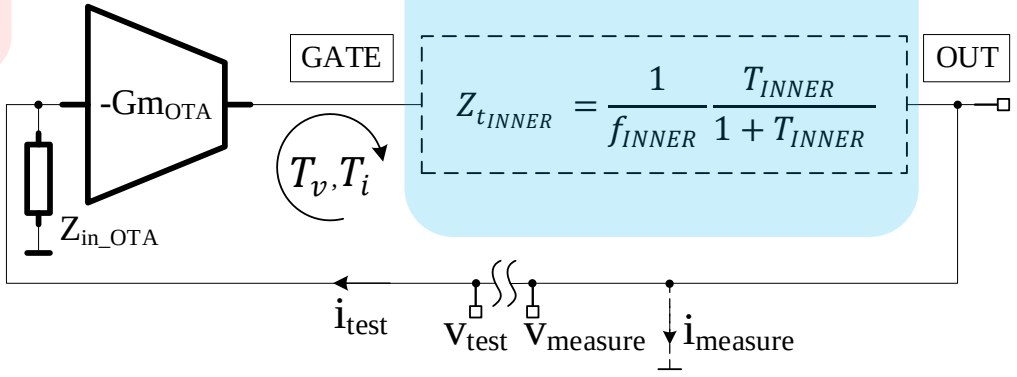
Low-power LDO with fast response to load transients
Stability Analysis

$$Gm_{F1} = Gm_{F2} = Gm_F$$
$$C1 = C2 = C$$
$$R1 = R2 = R$$





Classical Feedback Theory



$$T_{INNER} = \frac{2sRC(G_{mF}G_{mP}R_gR_L)}{(1+sR_gC_g)(1+sR_LC_L)(1+sRC)}$$

Low-power LDO with fast response to load transients
A graphical method for stability analysis

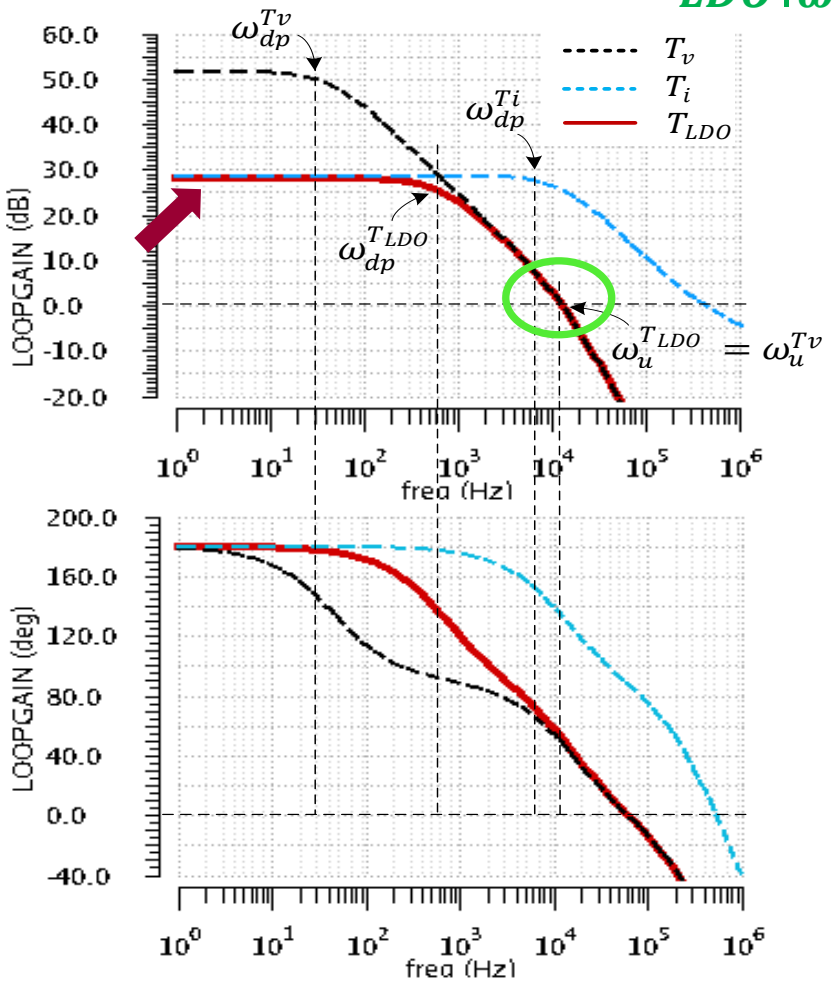
$$T_{LDO} = \frac{T_i T_v}{T_i + T_v} \leftarrow \text{" } T_i \parallel T_v \text{"}$$

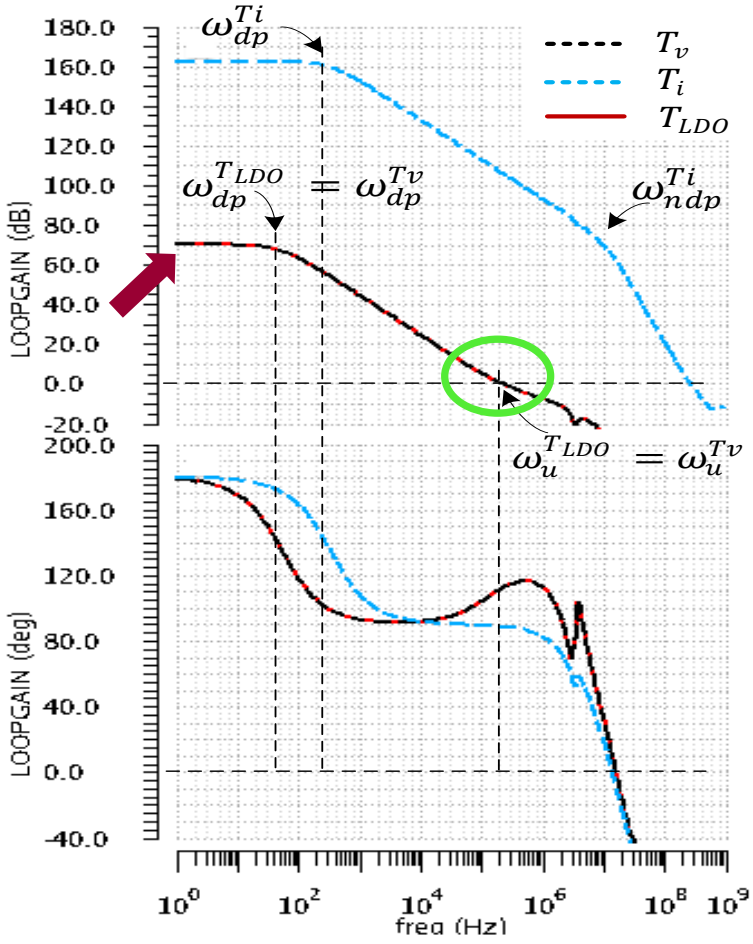
$$max\left\{\frac{C_L}{G_{mF}G_{mP}R_g}, \frac{C_g}{G_{mf}G_{mP}R_L}\right\} \leq RC \leq \sqrt{\frac{C_g C_L}{G_{mF}G_{mP}}}$$

T_LDO for small values of IL

$$T_{LDO}|_{\omega u} \cong T_v$$

T_LDO for large values of IL

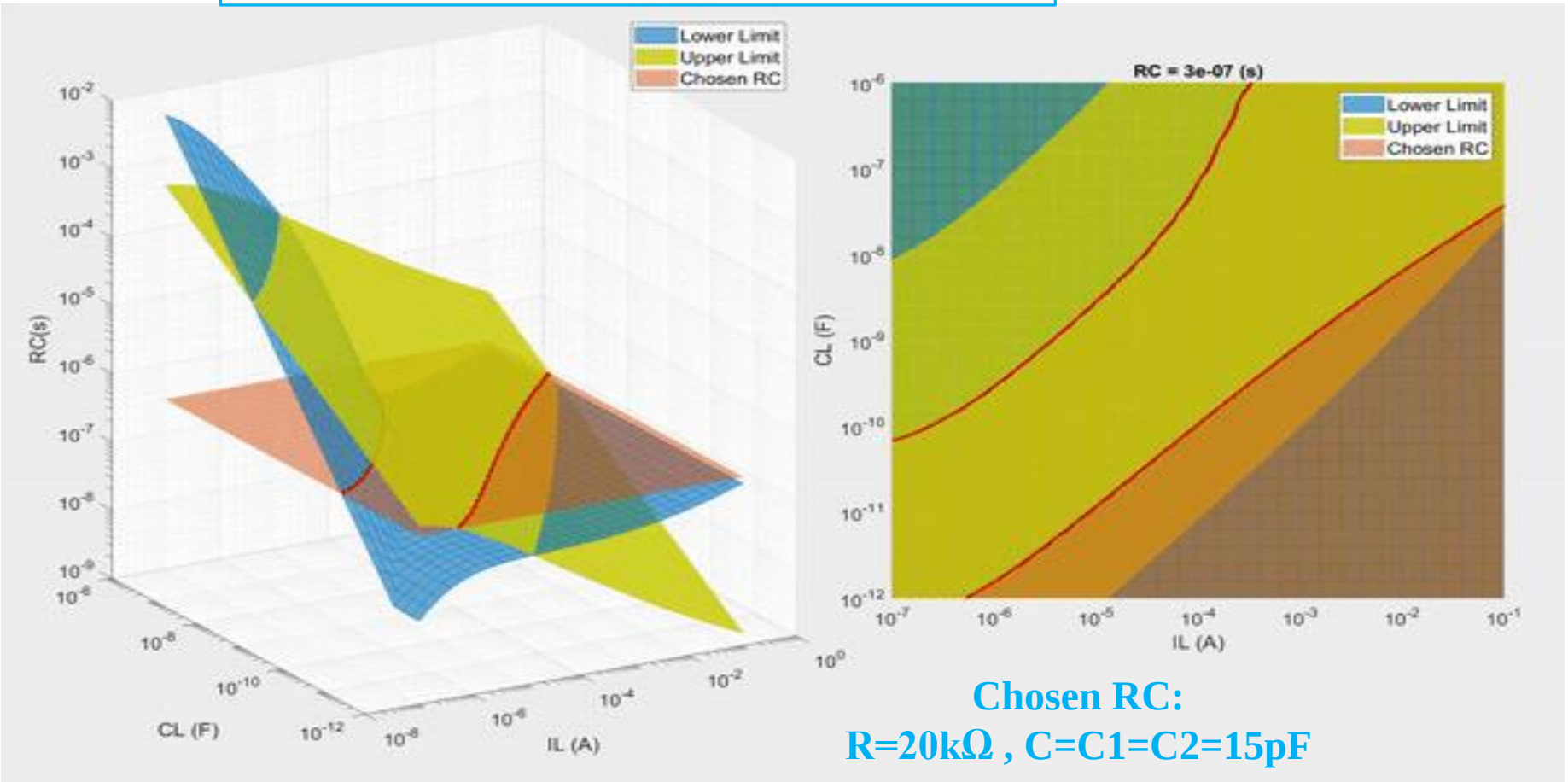




Low-power LDO with fast response to load transients
Sizing conditions for frequency compensation

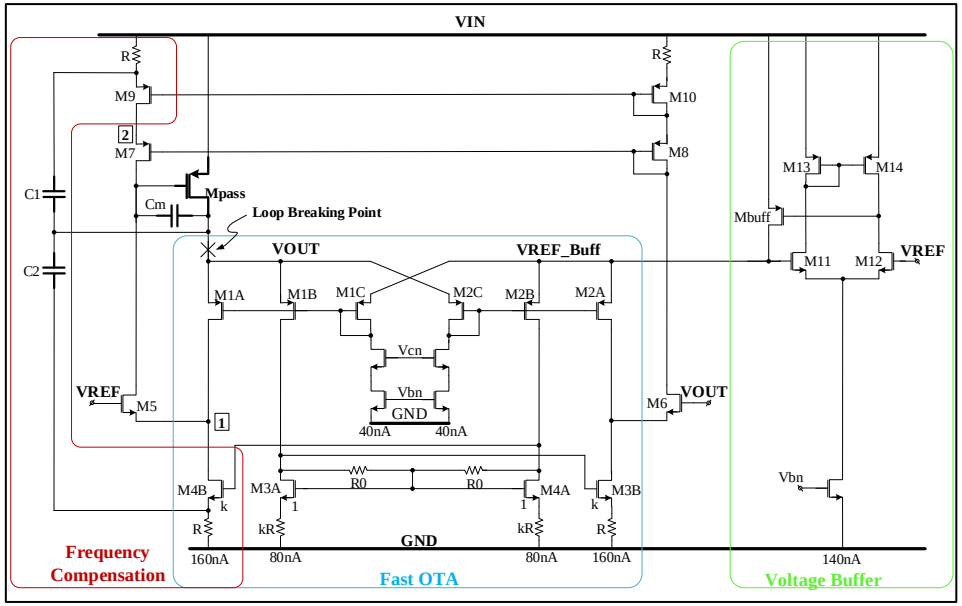
Lower Limit | Chosen RC | Upper Limit

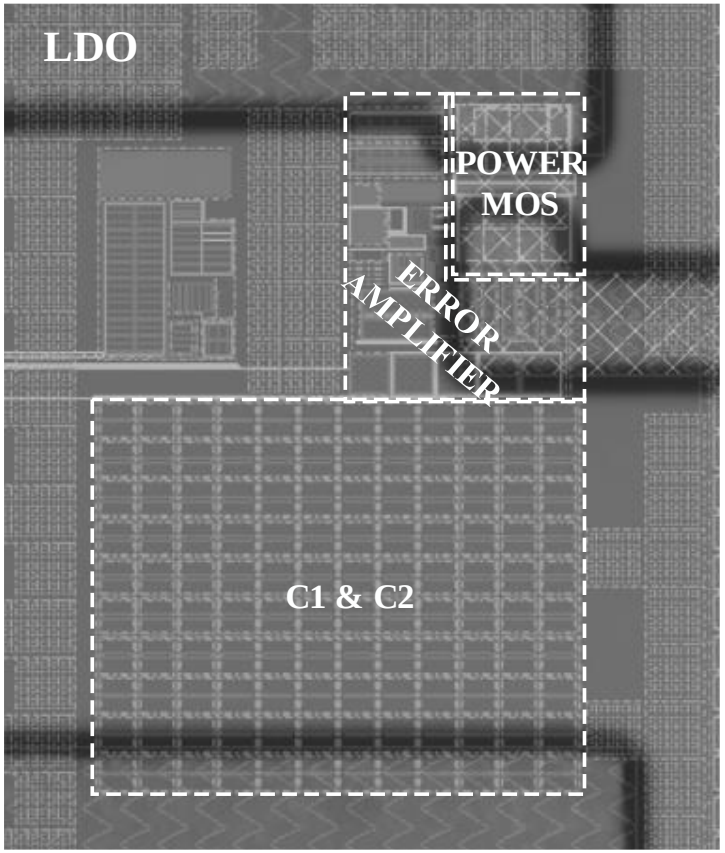
$$max\left\{\frac{C_L}{G_{mF}G_{mP}R_g}, \frac{C_g}{G_{mf}G_{mP}R_L}\right\} \leq RC \leq \sqrt{\frac{C_gC_L}{G_{mF}G_{mP}}}$$



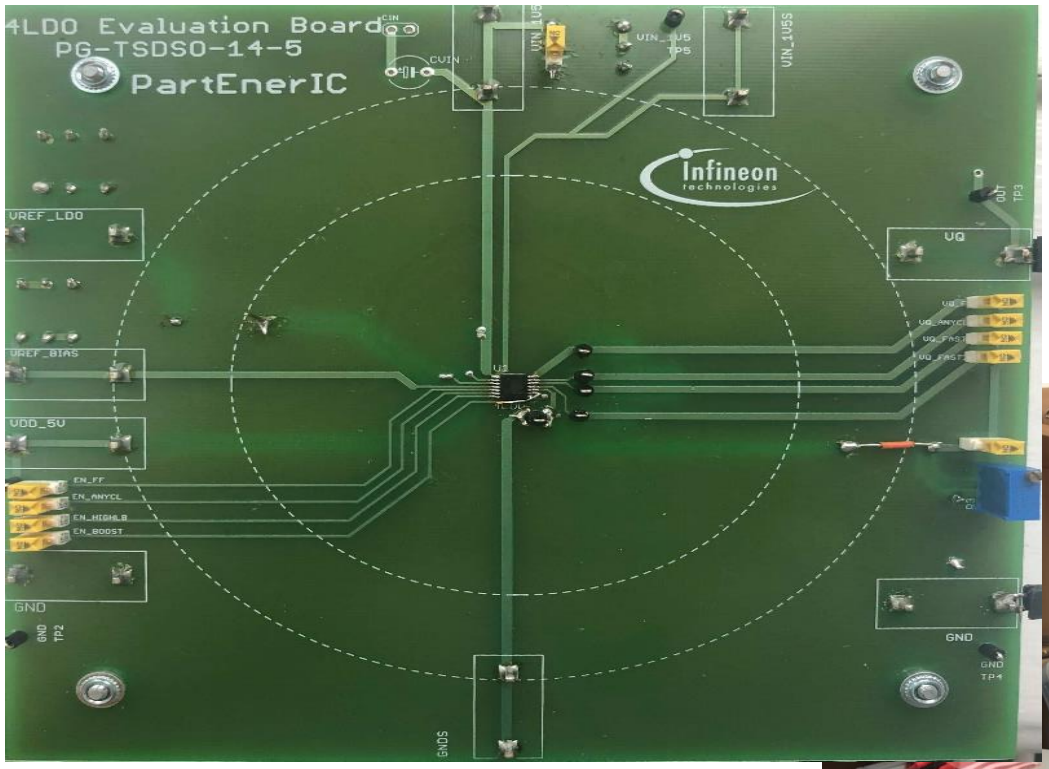
Chosen RC:
R=20kΩ , C=C1=C2=15pF

Low-power LDO with fast response to load transients
Silicon implementation



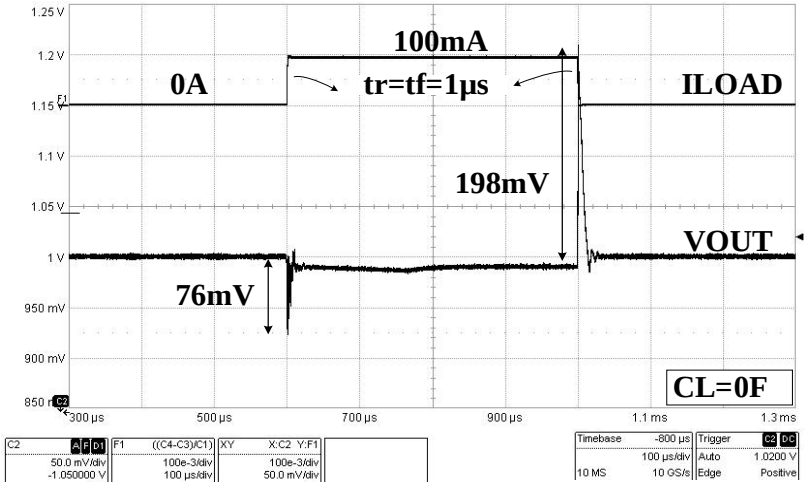


The PartEnerIC project: Ultra-low power LDO in 0.18um CMOS

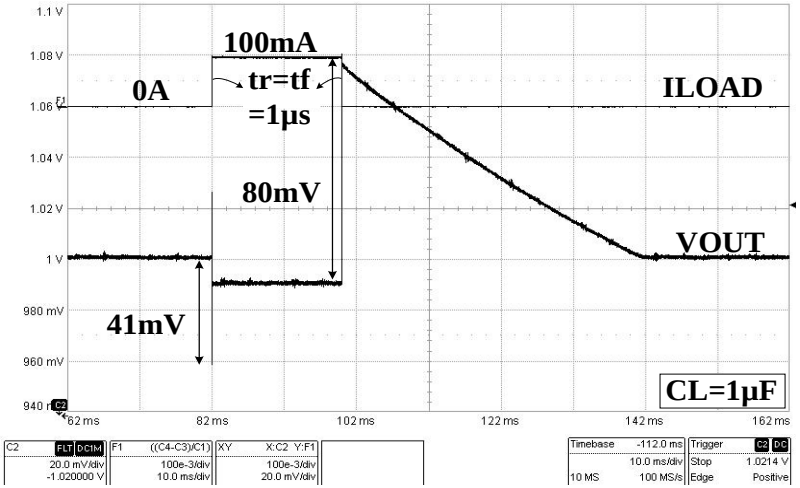


Ultra-low power LDO with fast response to load transients Measurement results

PARAMETER	[13]	[14]	This work
Year	2019	2020	2020
CMOS [um]	0.065	0.065	0.13
FO4Delay(ps)[c)]	17	17	35
Supply Voltage [V]	0.95-1.2	0.95-1.2	1.2-1.5
Output Voltage [V]	0.8	0.8	1
Dropout Voltage [mV]	150	150	100
Iq [µA]	13.9	14	**0.7**
DC Line Reg.[mV/V]	0.48	12	16.6
DC Load Reg. [µV/mA]	8.03	90	100
PSR [dB]	47@10kHz	33@10kHz	30@10kHz[d)]
CL [F]	0-100p	0-100p	**0-1µ**
ΔVout_pkpk= +ΔVout – (–ΔVout) [mV]	549	363	**200**
IL_{MIN} – IL_{MAX}	0-100mA	0-100mA	0-100mA
Avg. IL t_{rise} (ns)	50	132.5	1000
Rise time ratio (K)	1	2.65	20
FOM1 [fs]	7.63**	50.82	0.19**
FOM2 [mV]	0.08	0.13	0.04
FOM3 [V/µs]	4.49	4.14	0.15

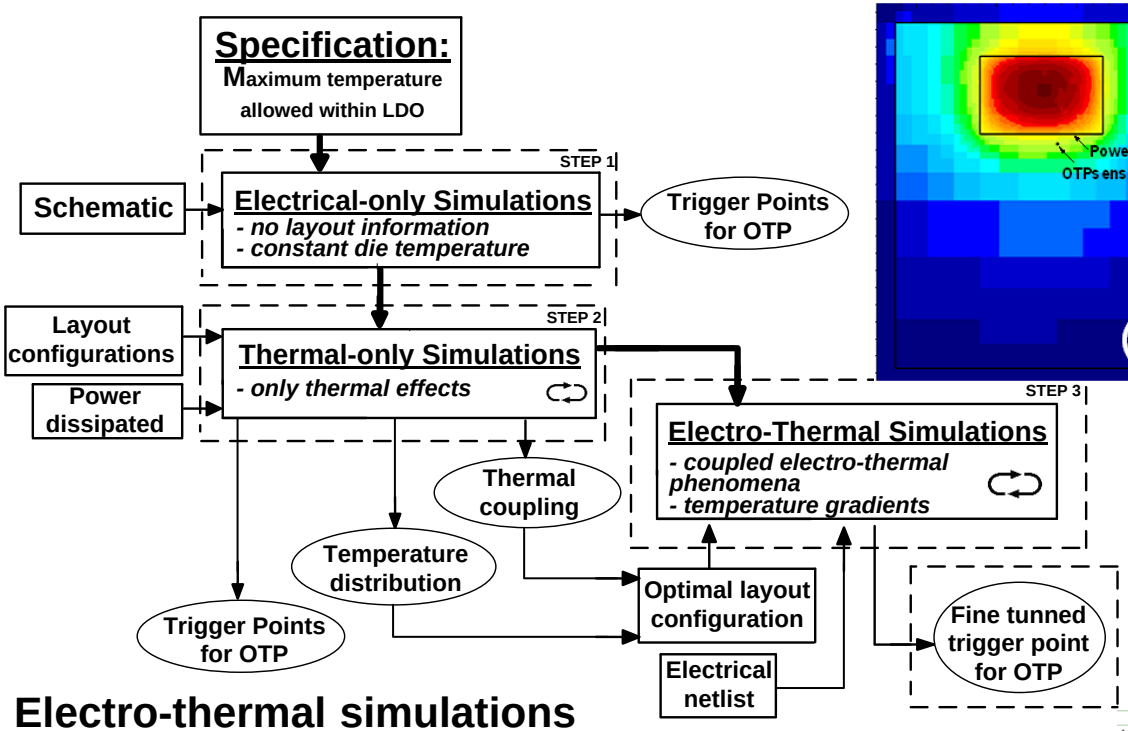


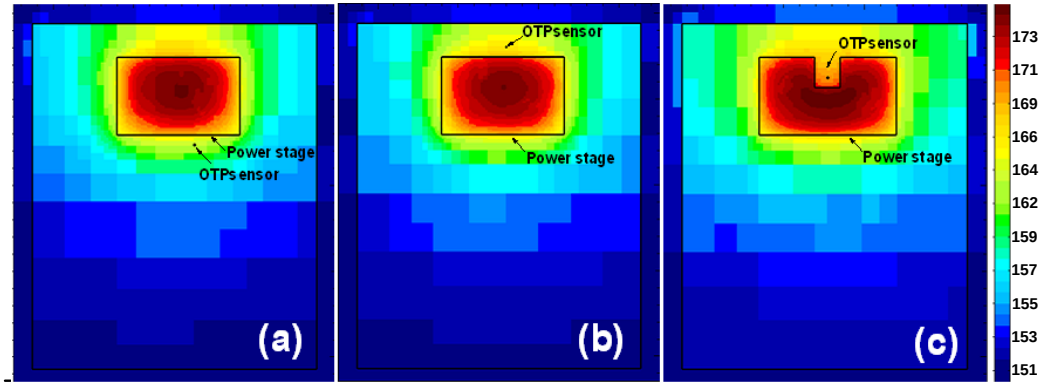
Measured response to a load step of 100mA in 1µs for VDD=1.5Vand CL=0F (plus 50pF from the scope probe)



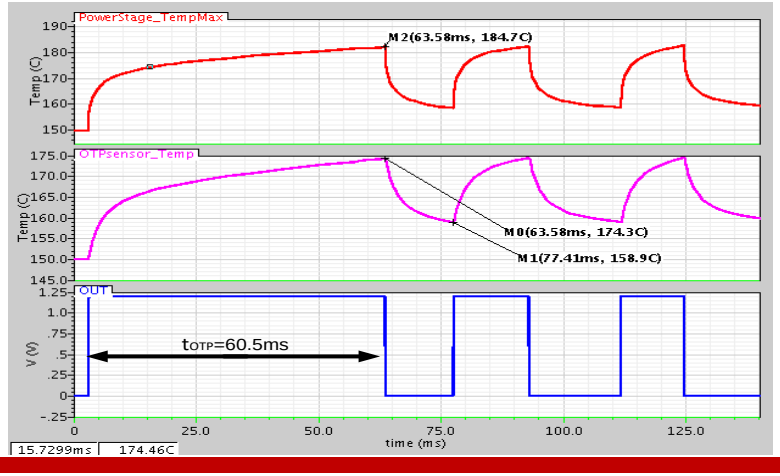
Measured response to a load step of 100mA in 1µs for VDD=1.5V and CL=1µF

Methodologies for designing over-current and over-temperature protection circuitry for PMICs

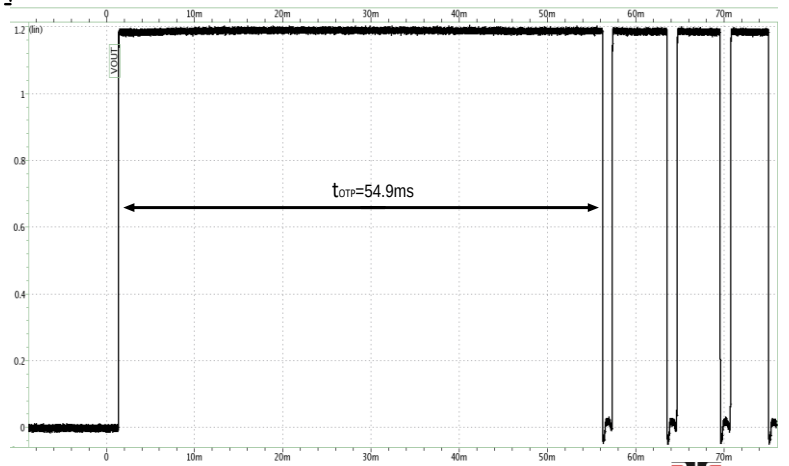




Electro-thermal simulations



Measurement results



Industry-funded projects 2021-2024

Advances in Data Science and Visualization

Aim: R&D for modeling the dependence of inline, process and electrical parameters measurements collected during the IC fabrication process

Duration: 1.5 years (2022-2023) **Team**: 1 professor, 1 post-doc, 2 PhD students

Main Results so far:

- Novel methodology for inline vs. process parameters correlation analysis
- New web-based big data analysis and report generation tool

High-performance Power Management Integrated Circuits

Aim: Development and validation of design methodologies for several types of LDOs, as well as support and control circuitry for linear and switched-mode regulators:

Duration: 3 years (2021-2024)

Team: 2 professors, 1 post-doc researcher, 3 PhD students, 1 master student

Main Results so far:

- Novel methodologies for stability analysis of LDOs with multiple feedback loops
- Novel topologies and design methodologies for LDOs for automotive applications

Plans for co-operation with industry in near future

- **National Plan for Recovery and Resilience (PNRR)**
  - TUCN was nominated (along with the TU in Bucharest, Iasi, Timisoara) as hosts for Centres of Excellence in Microelectronics

- **Important Project of Common European Interest (IPCEI) Microelectronics**
  - DERFAIC participates in two projects driven by Bosch Romania and NXP Romania

- **Direct engagements**
  - R&D consultancy projects
  - Training and tutoring on subjects outside the main curricula e.g. facultative course on “Systems with Analog IC for Automotive” sponsored by Infineon
  - Summer school + Internships within the DERFAIC group
  - Company-funded Scholarships for undergraduate & Master students

Contact us

EUROPEAN UNIVERSITY OF TECHNOLOGY

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